

UA78L Series Positive-Voltage Linear Regulators

1 Features

- Input voltage range (V_i): 4.75 V to 35 V
- Output voltage range (V_O):
 - 2.6 V to 15 V (for legacy chip)
 - 3.3 V to 15 V (for new chip)
- Output current: Up to 100 mA
- Quiescent current I_Q : 3.8 mA
- Built-in short-circuit current limiting and thermal protection
- Stable without any external component
- Supported temperature range:
 - Legacy chip C and AC versions: 0°C to +125°C
 - Legacy chip AI version: –40°C to +125°C
 - New chip: –40°C to +125°C
- Packages:
 - 8-pin, 4.9-mm × 3.91-mm SOIC
 - 3-pin, 4.3-mm × 4.3-mm TO-92
 - 3-pin, 4.5-mm × 2.5-mm SOT-89

2 Applications

- Motor drives
- Appliances
- Building automation
- Flow transmitters
- Factory automation and control

3 Description

The UA78L series of fixed-voltage linear regulators is designed for a wide range of applications. The UA78L series can be used for on-card regulation to eliminate the noise and distribution problems associated with single-point regulation. The UA78L can also be used with power-pass elements to make high-current voltage regulators. The UA78L series regulators can deliver up to 100 mA of output current. Additionally, the UA78L does not need an external capacitor for stable operation across the load current range. The internal current-limiting and thermal-shutdown features of these regulators help protect the device from overload.

For the legacy chip, the UA78L00C and UA78L00AC series are characterized for the junction temperature range of 0°C to +125°C and the UA78L05Ai device is characterized for the operating junction temperature range of –40°C to +125°C.

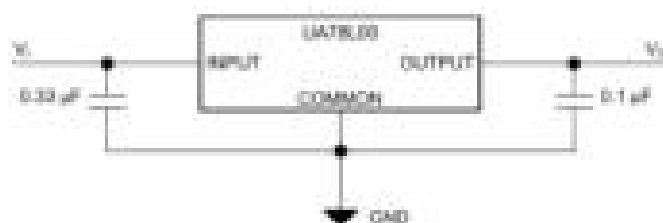
For the new chip, the UA78L series is characterized for the junction temperature range of –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
UA78L	D (SOIC, 8)	4.9 mm × 6 mm
	LP (TO-92, 3)	5.2 mm × 3.68 mm
	PK (SOT-89, 3)	4.5 mm × 4.095 mm

(1) For all available packages, see the orderable addendum at the end of this data sheet.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic



Table of Contents

1 Features	1	6.13 Electrical Characteristics: UA78L15 (Both Legacy and New Chip)	11
2 Applications	1	6.14 Typical Characteristics	13
3 Description	1	7 Detailed Description	17
4 Revision History	2	7.1 Overview	17
5 Pin Configuration and Functions	3	7.2 Functional Block Diagram	17
6 Specifications	4	7.3 Feature Description	17
6.1 Absolute Maximum Ratings.....	4	7.4 Device Functional Modes	19
6.2 ESD Ratings.....	4	8 Applications and Implementation	20
6.3 Recommended Operating Conditions.....	4	8.1 Application Information.....	20
6.4 Thermal Information.....	5	8.2 Typical Application.....	20
6.5 Electrical Characteristics: UA78L02 (Legacy Chip Only).....	6	8.3 System Examples.....	25
6.6 Electrical Characteristics: UA78L033 (New Chip Only).....	6	8.4 Power Supply Recommendations.....	25
6.7 Electrical Characteristics: UA78L05 (Both Legacy and New Chip).....	6	8.5 Layout.....	26
6.8 Electrical Characteristics: UA78L12 (Both Legacy and New Chip).....	7	9 Device and Documentation Support	27
6.9 Electrical Characteristics: UA78L06 (Legacy Chip Only).....	8	9.1 Device Support.....	27
6.10 Electrical Characteristics: UA78L08 (Legacy Chip Only).....	8	9.2 Receiving Notification of Documentation Updates.....	27
6.11 Electrical Characteristics: UA78L09 (Legacy Chip Only).....	9	9.3 Support Resources.....	27
6.12 Electrical Characteristics: UA78L10 (Legacy Chip Only).....	10	9.4 Trademarks.....	27
		9.5 Electrostatic Discharge Caution.....	27
		9.6 Glossary.....	27
		10 Mechanical, Packaging, and Orderable Information	27

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision W (April 2023) to Revision X (June 2023)	Page
• Changed M3 device status from <i>Advance Information</i> to <i>Production Data</i>	1
Changes from Revision V (November 2016) to Revision W (April 2023)	Page
• Added M3 devices to document.....	1
• Changed <i>Features</i> , <i>Applications</i> , and <i>Description</i> sections.....	1
• Changed <i>Description</i> column of <i>Pin Functions</i> table.....	3
• Added plots for new chip, reentered plots for legacy chip, and changed condition statement in <i>Typical Characteristics</i> section.....	13
• Changed <i>Overview</i> section.....	17
• Changed <i>Feature Description</i> section and added subsections.....	17
• Changed <i>Device Functional Modes</i> section: added <i>Device Functional Mode Comparison</i> table, deleted <i>Fixed-Output Mode</i> subsection, and added <i>Normal Operation</i> and <i>Dropout Operation</i> subsections.....	19
• Changed <i>Detailed Design Procedure</i> section and added subsections.....	20
• Added plots for new chip and changed condition statement in <i>Application Curves</i> section.....	24
• Added <i>Device Nomenclature</i> and <i>Evaluation Module</i> sections.....	27

5 Pin Configuration and Functions

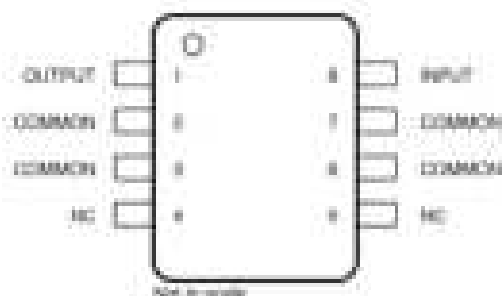


Figure 5-1. D Package, 8-Pin SOIC (Top View)



Figure 5-2. LP Package, 3-Pin TO-92 (Top View)

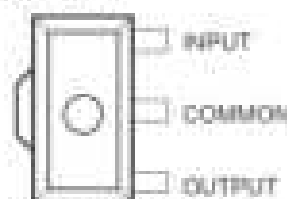


Figure 5-3. PK Package, 3-Pin SOT-69 (Top View)

NAME	PIN			TYPE	DESCRIPTION
	SOIC	TO-92	SOT-69		
COMMON	2, 3, 6, 7	2	2	—	Ground
INPUT	8	3	3	I	Input pin. Use the recommended capacitor value as listed in the Recommended Operating Conditions table. Place the input capacitor as close to the IN and GND pins of the device as possible.
OUTPUT	1	1	1	O	Output pin. Use the recommended capacitor value as listed in the Recommended Operating Conditions table. Place the output capacitor as close to the OUT and GND pins of the device as possible.
NC	4, 5	—	—	—	No connect pin. This pin is not connected internally. Connect this pin to ground for best thermal performance or leave floating.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage, V_i (for legacy chip)	UA78L00AC, UA78L00C, UA78L00AC, and UA78L10AC		30	V
	UA78L12C, UA78L12AC, UA78L15C, and UA78L15AC		30	
Input voltage, V_i (for new chip)	UA78L00A, UA78L00AC, UA78L00A, UA78L00C, UA78L12AC and UA78L15AC		45	
Junction temperature, T_j			150	°C
Storage temperature, T_{stg}		-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
V_{ESD}	Human body model (HBM), per ANSI/ESDA/IEC J5-001, all pins ⁽¹⁾	1000	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1000	1000	

- (1) JEDEC document JEP155 states that 100-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	TYP	MAX	UNIT
V_i	Input voltage	UA78L00AC (for legacy chip only)	4.75		25	V
		UA78L005AC (for new chip only)	4.75		25	
		UA78L00C and UA78L00AC (for both legacy and new chip)	7		30	
		UA78L00C and UA78L00AC (for legacy chip only)	6.5		25	
		UA78L00C and UA78L00AC (for legacy chip only)	10.5		25	
		UA78L00C and UA78L00AC (for legacy chip only)	11.5		24	
		UA78L10AC (for legacy chip only)	12.5		25	
		UA78L12C and UA78L12AC (for both legacy and new chip)	14.5		27	
		UA78L15C and UA78L15AC (for both legacy and new chip)	17.5		30	
I_o	Output current				100	mA
C_{in} ⁽²⁾	Input capacitor ⁽³⁾			0.33		μF
C_{out} ⁽⁴⁾	Output capacitor ⁽⁴⁾			0.1		
T_j	Operating junction temperature	UA78L00C and UA78L00AC series (for legacy chip)	0		125	°C
		UA78L00A (for legacy chip)	-40		125	
		UA78L00C / UA78L00AC, and UA78L00A series (for new chip)	-40		125	

- (1) All voltages are with respect to GND.

- (2) UA78L regulator doesn't need any external capacitors for the the LDO stability.

- (3) An input capacitor with value of 0.33 μF is recommended to counteract the effect of source resistance and inductance, which can in some cases cause symptoms of system level instability such as ringing or oscillation, especially in the presence of load transients.

- (4) An output capacitor with value of 0.1 μF is recommended to improve the load and line transient performance of the UA78L regulator.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		UA78L02			UNIT
		D (SOIC)	LP (TD-8)	PK (SOT-23)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110	143.8	54.7	°C/W
$R_{\theta JC(case)}$	Junction-to-case (typ) thermal resistance	80.3	74.4	88.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	85.8	—	9.8	°C/W
θ_{JA}	Junction-to-top characterization parameter	18.2	24.2	9.2	°C/W
θ_{JB}	Junction-to-board characterization parameter	85	120.8	9.7	°C/W
$R_{\theta JC(case)}$	Junction-to-case (bottom) thermal resistance	—	—	7.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: UA78L02 (Legacy Chip Only)

at specified junction temperature, $V_I = 9\text{ V}$, $C_{IN} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾	MIN	TYP	MAX	UNIT
Output voltage	$V_I = 4.75\text{ V}$ to 20 V and $I_O = 1\text{ mA}$ to 40 mA	2.5	2.8	2.7	V
	$T_J = 25^\circ\text{C}$				
	$T_J = 0^\circ\text{C}$ to 125°C				
Input voltage regulation	$I_O = 1\text{ mA}$ to 75 mA , and $T_J = 0^\circ\text{C}$ to 125°C	2.45	—	2.75	mV
	$V_I = 4.75\text{ V}$ to 20 V and $T_J = 25^\circ\text{C}$				
	$V_I = 8\text{ V}$ to 20 V , and $T_J = 25^\circ\text{C}$				
Reggie rejection	$V_I = 8\text{ V}$ to 20 V , $f = 120\text{ Hz}$, and $T_J = 25^\circ\text{C}$	43	51	—	dB
Output voltage regulation	$I_O = 1\text{ mA}$ to 100 mA , and $T_J = 25^\circ\text{C}$	12	—	80	mV
	$I_O = 1\text{ mA}$ to 40 mA , and $T_J = 25^\circ\text{C}$				
Output noise voltage	$f = 50\text{ mHz}$ to 100 kHz , and $T_J = 25^\circ\text{C}$	—	30	—	μV
Dropout voltage	$T_J = 25^\circ\text{C}$	—	1.7	—	V
Bias current	$T_J = 25^\circ\text{C}$	—	3.0	8	nA
	$T_J = 100^\circ\text{C}$				
Bias current change	$V_I = 8\text{ V}$ to 20 V , and $T_J = 0^\circ\text{C}$ to 125°C	—	—	1.0	nA
	$I_O = 1\text{ mA}$ to 40 mA , and $T_J = 0^\circ\text{C}$ to 125°C				

(1) Applies to UA78L02AC.

(2) Pulsed-loading techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L02AC is $T_J = 0^\circ\text{C}$ to 125°C .

6.6 Electrical Characteristics: UA78L033 (New Chip Only)

at specified junction temperature, $V_I = 9\text{ V}$, $C_{IN} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾	MIN	TYP	MAX	UNIT
Output voltage	$V_I = 3.0\text{ V}$ to 20 V , and $I_O = 1\text{ mA}$ to 40 mA , $T_J = 25^\circ\text{C}$	3.28	3.3	3.44	V
	$V_I = 3.0\text{ V}$ to 20 V , and $I_O = 1\text{ mA}$ to 40 mA , $T_J = 40^\circ\text{C}$ to 125°C				
	$I_O = 1\text{ mA}$ to 75 mA , $T_J = -40^\circ\text{C}$ to 125°C				
Input voltage regulation	$V_I = 3.0\text{ V}$ to 20 V , and $T_J = 25^\circ\text{C}$	19	23	—	mV
	$V_I = 8\text{ V}$ to 20 V , and $T_J = 25^\circ\text{C}$				
Reggie rejection	$V_I = 8\text{ V}$ to 20 V , $f = 120\text{ Hz}$, and $T_J = 25^\circ\text{C}$	48	57.3	—	dB
Output voltage regulation	$I_O = 1\text{ mA}$ to 100 mA , and $T_J = 25^\circ\text{C}$	13.3	—	28	mV
	$I_O = 1\text{ mA}$ to 40 mA , and $T_J = 25^\circ\text{C}$				
Output noise voltage	$f = 50\text{ mHz}$ to 100 kHz , and $T_J = 25^\circ\text{C}$	—	60	—	μV
Dropout voltage	$T_J = 25^\circ\text{C}$	—	1.7	—	V

6.6 Electrical Characteristics: UA78L033 (New Chip Only) (continued)

at specified junction temperature, $V_i = 9\text{ V}$, $C_{DS} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾	MIN	TYP	MAX	UNIT
Rise current	$T_J = 25^\circ\text{C}$		3.53	4.1	mA
	$T_J = 125^\circ\text{C}$			4.1	
Rise current change	$V_i = 8\text{ V to }25\text{ V}$, and $T_J = -40^\circ\text{C to }125^\circ\text{C}$			0.07%	mA
	$I_O = 1\text{ mA to }40\text{ mA}$, and $T_J = -40^\circ\text{C to }125^\circ\text{C}$			0.07	

(1) Applies to UA78L033.

(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately.

6.7 Electrical Characteristics: UA78L05 (Both Legacy and New Chip)

at specified junction temperature, $V_i = 10\text{ V}$, $C_{DS} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾			MIN	TYP	MAX	UNIT
Output voltage	$V_i = 7\text{ V to }25\text{ V}$, and $I_o = 1\text{ mA to }40\text{ mA}$ (for legacy chip)	$T_j = 25^\circ\text{C}$	UA78L05C	4.8	5	5.4	V
			UA78L05AC and UA78L05AI	4.8	5	5.3	
		$T_j = \text{full range}$	UA78L05C	4.5		5.0	
			UA78L05AC and UA78L05AI	4.75		5.25	
		$I_o = 1\text{ mA to }70\text{ mA}$, and $T_j = \text{full range}$ (for legacy chip)	UA78L05C	4.5		5.0	
			UA78L05AC and UA78L05AI	4.75		5.25	
	$V_i = 7\text{ V to }25\text{ V}$, and $I_o = 1\text{ mA to }40\text{ mA}$ (for new chip)	$T_j = 25^\circ\text{C}$	UA78L05C	4.95	5	5.15	
			UA78L05AC and UA78L05AI	4.95	5	5.15	
		$T_j = \text{full range}$	UA78L05C	4.85		5.15	
			UA78L05AC and UA78L05AI	4.95		5.15	
		$I_o = 1\text{ mA to }70\text{ mA}$, and $T_j = \text{full range}$ (for new chip)	UA78L05C	4.95		5.15	
			UA78L05AC and UA78L05AI	4.95		5.15	
Input voltage regulation	$V_i = 7\text{ V to }25\text{ V}$, and $T_j = 25^\circ\text{C}$ (for legacy chip)	UA78L05C		32	200	mV	
	UA78L05AC and UA78L05AI		32	100			
	$V_i = 8\text{ V to }25\text{ V}$, and $T_j = 25^\circ\text{C}$ (for legacy chip)	UA78L05C		28	100		
	UA78L05AC and UA78L05AI		26	100			
	$V_i = 7\text{ V to }25\text{ V}$, and $T_j = 25^\circ\text{C}$ (for new chip)	UA78L05C		32	32		
	UA78L05AC and UA78L05AI		32	32			
	$V_i = 8\text{ V to }25\text{ V}$, and $T_j = 25^\circ\text{C}$ (for new chip)	UA78L05C		26	26		
	UA78L05AC and UA78L05AI		26	26			
Regain rejection	$V_i = 8\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$, and $T_j = 25^\circ\text{C}$ (for legacy chip)	UA78L05C	40	40	dB		
		UA78L05AC and UA78L05AI	41	40			
	$V_i = 8\text{ V to }18\text{ V}$, $f = 120\text{ Hz}$, and $T_j = 25^\circ\text{C}$ (for new chip)	UA78L05C	48	55			
		UA78L05AC and UA78L05AI	48	55			
Output voltage regulation	for legacy chip	$I_o = 1\text{ mA to }100\text{ mA}$, and $T_j = 25^\circ\text{C}$		15	60	mV	
		$I_o = 1\text{ mA to }40\text{ mA}$, and $T_j = 25^\circ\text{C}$		8	30		
	for new chip	$I_o = 1\text{ mA to }100\text{ mA}$, and $T_j = 25^\circ\text{C}$		15	35		
		$I_o = 1\text{ mA to }40\text{ mA}$, and $T_j = 25^\circ\text{C}$		8	15		
Output noise voltage	for legacy chip	$f = 10\text{ Hz to }100\text{ kHz}$, and $T_j = 25^\circ\text{C}$		40	μV		
	for new chip	$f = 10\text{ Hz to }100\text{ kHz}$, and $T_j = 25^\circ\text{C}$		125			
Dropout voltage	for legacy chip	$T_j = 25^\circ\text{C}$		1.7	V		
	for new chip	$T_j = 25^\circ\text{C}$		1.7	V		

6.7 Electrical Characteristics: UA78L05 (Both Legacy and New Chip) (continued)

at specified junction temperature, $V_i = 10\text{ V}$, $C_{in} = 0.33\text{ }\mu\text{F}$, $C_{out} = 0.1\text{ }\mu\text{F}$ and $I_o = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾		MIN	TYP	MAX	UNIT
Bias current	for legacy chip	$T_j = 25^\circ\text{C}$		3.8	6	mA
		$T_j = 125^\circ\text{C}$			5.5	mA
	for new chip	$T_j = 25^\circ\text{C}$		3.52	3.95	mA
		$T_j = 125^\circ\text{C}$			4.0	mA
Bias current change	$V_i = 8\text{ V}$ to 27 V , and $T_j = \text{full range}$ (for new legacy chip)				1.5	mA
	$I_o = 1\text{ mA}$ to 40 mA , and $T_j = \text{full range}$ (for legacy chip)	UA78L05C			1.5	mA
		UA78L05AC and UA78L05AJ			1.5	mA
	$V_i = 8\text{ V}$ to 27 V , and $T_j = \text{full range}$ (for new chip)				0.488	
	$I_o = 1\text{ mA}$ to 40 mA , and $T_j = \text{full range}$ (for new chip)	UA78L05C			0.31	mA
		UA78L05AC and UA78L05AJ			0.31	

(1) Applies to UA78L05C, UA78L05AC and UA78L05AJ.

(2) Pulse-testing techniques maintain T_j as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L05C, UA78L05AC is $T_j = 0^\circ\text{C}$ to 125°C , and for the UA78L05AJ is $T_j = -40^\circ\text{C}$ to 125°C . For new chip, temperature range for the UA78L05C, UA78L05AC and UA78L05AJ is $T_j = -40^\circ\text{C}$ to 125°C .

6.8 Electrical Characteristics: UA78L12 (Both Legacy and New Chip)

at specified junction temperature, $V_i = 19\text{ V}$, $C_{in} = 0.33\text{ }\mu\text{F}$, $C_{out} = 0.1\text{ }\mu\text{F}$ and $I_o = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾			MIN	TYP	MAX	UNIT
Output voltage	$V_i = 14\text{ V}$ to 27 V , and $I_o = 1\text{ mA}$ to 40 mA	$T_j = 25^\circ\text{C}$	UA78L12C (legacy chip)	11.1	12	12.9	V
			UA78L12AC (legacy chip)	11.5	12	12.5	
		$T_j = 0^\circ\text{C}$ to 125°C	UA78L12C (legacy chip)	10.8		12.2	
			UA78L12AC (legacy chip)	11.4		12.8	
		$T_j = 0^\circ\text{C}$ to 125°C , and $I_o = 1\text{ mA}$ to 75 mA	UA78L12C (legacy chip)	10.8		13.2	
			UA78L12AC (legacy chip)	11.4		12.9	
	$V_i = 14\text{ V}$ to 27 V , and $I_o = 1\text{ mA}$ to 40 mA	$T_j = 25^\circ\text{C}$	UA78L12C (new chip)	11.83	12	12.31	
			UA78L12AC (new chip)				
		$T_j = -40^\circ\text{C}$ to 125°C	UA78L12C (new chip)	11.85		12.38	
			UA78L12AC (new chip)				
		$T_j = -40^\circ\text{C}$ to 125°C , and $I_o = 1\text{ mA}$ to 75 mA	UA78L12C (new chip)	11.47		12.38	
			UA78L12AC (new chip)				
Input voltage regulation	$T_j = 25^\circ\text{C}$	$V_i = 14.5\text{ V}$ to 27 V	for legacy chip		68	250	mV
		$V_i = 18\text{ V}$ to 27 V			48	200	
		$V_i = 14.5\text{ V}$ to 27 V	for new chip		68	80	
		$V_i = 18\text{ V}$ to 27 V			48	66	
Ripple rejection	$T_j = 25^\circ\text{C}$	$V_i = 18\text{ V}$ to 28 V , and $f = 120\text{ Hz}$	UA78L12C (legacy chip)	36	42		dB
			UA78L12AC (legacy chip)	37	42		
			UA78L12C (new chip)				
			UA78L12AC (new chip)	40	58		

6.8 Electrical Characteristics: UA78L12 (Both Legacy and New Chip) (continued)

at specified junction temperature, $V_i = 18\text{ V}$, $C_{in} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾		MIN	TYP	MAX	UNIT
Output voltage regulation	$T_J = 25^\circ\text{C}$	$I_O = 1\text{ mA to }100\text{ mA}$	for legacy chip	22	100	mV
		$I_O = 1\text{ mA to }40\text{ mA}$		13	80	
		$I_O = 1\text{ mA to }100\text{ mA}$	for new chip	22	70	
		$I_O = 1\text{ mA to }40\text{ mA}$		13	30	
Output noise voltage	$T_J = 25^\circ\text{C}$, and $f = 10\text{ Hz to }100\text{ kHz}$	for legacy chip		16		μV
		for new chip		280		μV
Dropout voltage	$T_J = 25^\circ\text{C}$	for legacy chip		1.7		V
		for new chip		1.3		
Bias current	$T_J = 25^\circ\text{C}$	for legacy chip		4.3	5.5	mA
	$T_J = 125^\circ\text{C}$				6	
	$T_J = 25^\circ\text{C}$	for new chip		0.94	4.300	mA
	$T_J = 125^\circ\text{C}$				4.300	
Bias current change	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	$V_i = 18\text{ V to }27\text{ V (legacy chip)}$			1.5	mA
		$I_O = 1\text{ mA to }40\text{ mA}$	UA78L12C (legacy chip)		0.2	
			UA78L12AC (legacy chip)		0.1	
		$V_i = 18\text{ V to }27\text{ V (new chip)}$			0.480	
	$T_J = -40^\circ\text{C to }125^\circ\text{C}$	$I_O = 1\text{ mA to }40\text{ mA}$	UA78L12C (new chip)			
			UA78L12AC (new chip)		0.03	

(1) Applies to UA78L12C and UA78L12AC.

(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L12C, UA78L12AC is $T_J = 0^\circ\text{C to }125^\circ\text{C}$. For new chip, temperature range for the UA78L12C and UA78L12AC is $T_J = -40^\circ\text{C to }125^\circ\text{C}$.

6.9 Electrical Characteristics: UA78L06 (Legacy Chip Only)

at specified junction temperature, $V_i = 12\text{ V}$, $C_{in} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾		MIN	TYP	MAX	UNIT	
Output voltage	$V_i = 8.5\text{ V to }20\text{ V}$ $I_O = 1\text{ mA to }40\text{ mA}$	$T_J = 25^\circ\text{C}$	UA78L06C	5.7	6.2	6.7	V
			UA78L06AC	5.95	6.2	6.45	
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	UA78L06C			6.8	
			UA78L06AC			6.8	
	$T_J = 0^\circ\text{C to }125^\circ\text{C}$, and $I_O = 1\text{ mA to }70\text{ mA}$		UA78L06C			6.8	
			UA78L06AC			6.8	
Input voltage regulation	$T_J = 25^\circ\text{C}$	$V_i = 8.5\text{ V to }20\text{ V}$	UA78L06C		85	100	mV
			UA78L06AC		30	170	
		$V_i = 8\text{ V to }20\text{ V}$	UA78L06C		29	150	
			UA78L06AC		29	120	
Ripple rejection	$T_J = 25^\circ\text{C}$, $V_i = 10\text{ V to }20\text{ V}$, and $f = 120\text{ Hz}$		UA78L06C	38	40		dB
			UA78L06AC	60	60		
Output voltage regulation	$T_J = 25^\circ\text{C}$	$I_O = 1\text{ mA to }100\text{ mA}$		50	80	mV	
		$I_O = 1\text{ mA to }40\text{ mA}$		9	40		
Output noise voltage	$T_J = 25^\circ\text{C}$, and $f = 10\text{ Hz to }100\text{ kHz}$			40		μV	
Dropout voltage	$T_J = 25^\circ\text{C}$			1.7		V	
Bias current	$T_J = 25^\circ\text{C}$			0.8	6	mA	
	$T_J = 125^\circ\text{C}$				0.8		

6.9 Electrical Characteristics: UA78L06 (Legacy Chip Only) (continued)

at specified junction temperature, $V_i = 12\text{ V}$, $C_{IN} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾		MIN	TYP	MAX	UNIT
Rise current change	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	$V_i = 9\text{ V to }25\text{ V}$			1.5	
		$I_O = 1\text{ mA to }40\text{ mA}$	UA78L06C		0.2	mA
			UA78L06AC		0.1	

(1) Applies to UA78L06C and UA78L06AC.

(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L06C and UA78L06AC is $T_J = 0^\circ\text{C to }125^\circ\text{C}$.

6.10 Electrical Characteristics: UA78L08 (Legacy Chip Only)

at specified junction temperature, $V_i = 14\text{ V}$, $C_{IN} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾		MIN	TYP	MAX	UNIT
Output voltage	$V_i = 10.5\text{ V to }23\text{ V}$ $I_O = 1\text{ mA to }40\text{ mA}$	$T_J = 25^\circ\text{C}$	UA78L08C	7.35	8	V
			UA78L08AC	7.2	8	
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	UA78L08C	7.2	8.5	
			UA78L08AC	7.6	8.4	
	$I_O = 1\text{ mA to }70\text{ mA}$	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	UA78L08C	7.2	8.8	
			UA78L08AC	7.8	8.4	
Input voltage regulation	$T_J = 25^\circ\text{C}$	$V_i = 10.5\text{ V to }23\text{ V}$	UA78L08C		42	mV
			UA78L08AC		42	
		$V_i = 11\text{ V to }23\text{ V}$	UA78L08C		39	
			UA78L08AC		35	
Ripple rejection	$V_i = 12\text{ V to }23\text{ V}$, $f = 120\text{ Hz}$, and $T_J = 25^\circ\text{C}$	UA78L08C	38	45		dB
		UA78L08AC	37	45		
Output voltage regulation	$T_J = 25^\circ\text{C}$	$I_O = 1\text{ mA to }100\text{ mA}$		15	80	mV
		$I_O = 1\text{ mA to }40\text{ mA}$		10	45	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$, and $T_J = 25^\circ\text{C}$			54		μV
Dropout voltage	$T_J = 25^\circ\text{C}$			1.7		V
Rise current	$T_J = 25^\circ\text{C}$			8	9	mA
	$T_J = 125^\circ\text{C}$				0.3	
Rise current change	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	$V_i = 11\text{ V to }23\text{ V}$			1.5	mA
		$I_O = 1\text{ mA to }40\text{ mA}$	UA78L08C		0.2	
			UA78L08AC		0.1	

(1) Applies to UA78L08C and UA78L08AC.

(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L08C and UA78L08AC is $T_J = 0^\circ\text{C to }125^\circ\text{C}$.

6.11 Electrical Characteristics: UA78L09 (Legacy Chip Only)

at specified junction temperature, $V_i = 16\text{ V}$, $C_{IN} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾		MIN	TYP	MAX	UNIT
Output voltage	$V_i = 12\text{ V to }34\text{ V}$ $I_O = 1\text{ mA to }40\text{ mA}$	$T_J = 25^\circ\text{C}$	UA78L09C	9.2	9	V
			UA78L09AC	9.8	9	
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	UA78L09C	9.1	9.9	
			UA78L09AC	9.55	9.45	
	$I_O = 1\text{ mA to }70\text{ mA}$, and $T_J = 0^\circ\text{C to }125^\circ\text{C}$	UA78L09C	9.1		9.9	
		UA78L09AC	9.55		9.45	
Input voltage regulation	$T_J = 25^\circ\text{C}$	$V_i = 12\text{ V to }34\text{ V}$	UA78L09C		45	mV
			UA78L09AC		45	
		$V_i = 13\text{ V to }34\text{ V}$	UA78L09C		40	
			UA78L09AC		40	

6.11 Electrical Characteristics: UA78L09 (Legacy Chip Only) (continued)

at specified junction temperature, $V_i = 15\text{ V}$, $C_{in} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾		MIN	TYP	MAX	UNIT
Ripple rejection	$V_i = 15\text{ V to }25\text{ V}$, $f = 120\text{ Hz}$, and $T_J = 25^\circ\text{C}$	UA78L09C	38	45		dB
		UA78L09AC	38	45		
Output voltage regulation	$T_J = 25^\circ\text{C}$	$I_O = 1\text{ mA to }100\text{ mA}$		19	80	mV
		$I_O = 1\text{ mA to }40\text{ mA}$		11	40	
Output noise voltage	$f = 10\text{ Hz to }100\text{ kHz}$, and $T_J = 25^\circ\text{C}$			68		μV
Dropout voltage	$T_J = 25^\circ\text{C}$			1.7		V
Bias current	$T_J = 25^\circ\text{C}$			4.1	8	mA
	$T_J = 125^\circ\text{C}$				9.0	
Bias current change	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	$V_i = 15\text{ V to }24\text{ V}$			1.5	mA
		$I_O = 1\text{ mA to }40\text{ mA}$	UA78L09C		0.2	
			UA78L09AC		0.1	

(1) Applies to UA78L09C and UA78L09AC.

(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L09C and UA78L09AC is $T_J = 0^\circ\text{C to }125^\circ\text{C}$.

6.12 Electrical Characteristics: UA78L10 (Legacy Chip Only)

at specified junction temperature, $V_i = 14\text{ V}$, $C_{in} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾		MIN	TYP	MAX	UNIT
Output voltage	$V_i = 13\text{ V to }25\text{ V}$, and $I_O = 1\text{ mA to }40\text{ mA}$	$T_J = 25^\circ\text{C}$	9.8	10	10.4	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	9.5		10.5	
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$, and $I_O = 1\text{ mA to }75\text{ mA}$	9.5		10.5	
Input voltage regulation	$T_J = 25^\circ\text{C}$	$V_i = 13\text{ V to }25\text{ V}$		51	175	mV
		$V_i = 14\text{ V to }25\text{ V}$		42	125	
Ripple rejection	$T_J = 25^\circ\text{C}$, $V_i = 15\text{ V to }25\text{ V}$, and $f = 120\text{ Hz}$		37	44		dB
Output voltage regulation	$T_J = 25^\circ\text{C}$	$I_O = 1\text{ mA to }100\text{ mA}$		38	80	mV
		$I_O = 1\text{ mA to }40\text{ mA}$		11	40	
Output noise voltage	$T_J = 25^\circ\text{C}$, and $f = 10\text{ Hz to }100\text{ kHz}$			60		μV
Dropout voltage	$T_J = 25^\circ\text{C}$			1.7		V
Bias current	$T_J = 25^\circ\text{C}$			4.2	8	mA
	$T_J = 125^\circ\text{C}$				9.0	
Bias current change	$T_J = 0^\circ\text{C to }125^\circ\text{C}$	$V_i = 14\text{ V to }25\text{ V}$			1.8	mA
		$I_O = 1\text{ mA to }40\text{ mA}$			0.1	

(1) Applies to UA78L10AC.

(2) Pulse-testing techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L10AC is $T_J = 0^\circ\text{C to }125^\circ\text{C}$.

6.13 Electrical Characteristics: UA78L15 (Both Legacy and New Chip)

at specified junction temperature, $V_I = 20\text{ V}$, $C_{AQ} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾			MIN	TYP	MAX	UNIT
Output voltage	$V_I = 17.5\text{ V to }20\text{ V}$, and $I_O = 1\text{ mA to }40\text{ mA}$	$T_J = 25^\circ\text{C}$	UA78L15C (legacy chip)	13.2	15	16.2	V
			UA78L15AC (legacy chip)	14.4	15	16.6	V
		$T_J = 0^\circ\text{C to }125^\circ\text{C}$	UA78L15C (legacy chip)	13.2		16.2	V
			UA78L15AC (legacy chip)	14.25		16.75	V
	$T_J = 0^\circ\text{C to }125^\circ\text{C}$, and $I_O = 1\text{ mA to }70\text{ mA}$		UA78L15C (legacy chip)	13.5		16.5	V
			UA78L15AC (legacy chip)	14.25		16.75	V
	$V_I = 17.5\text{ V to }20\text{ V}$, and $I_O = 1\text{ mA to }40\text{ mA}$	$T_J = 25^\circ\text{C}$	UA78L15C (new chip)	14.750	15	15.425	V
			UA78L15AC (new chip)	14.750	15	15.425	
		$T_J = -40^\circ\text{C to }125^\circ\text{C}$	UA78L15C (new chip)	14.575		15.450	
			UA78L15AC (new chip)	14.575		15.450	
	$T_J = -40^\circ\text{C to }125^\circ\text{C}$, and $I_O = 1\text{ mA to }70\text{ mA}$		UA78L15C (new chip)	14.25		15.45	V
			UA78L15AC (new chip)	14.25		15.45	
Input voltage regulation	$T_J = 25^\circ\text{C}$	$V_I = 17.5\text{ V to }20\text{ V}$	for legacy chip		85	100	mV
		$V_I = 20\text{ V to }30\text{ V}$			90	100	
		$V_I = 17.5\text{ V to }20\text{ V}$	for new chip		85	92	
		$V_I = 20\text{ V to }30\text{ V}$			90	93	
Ripple rejection	$T_J = 25^\circ\text{C}$	$V_I = 18.5\text{ V to }28.5\text{ V}$, and $f = 120\text{ Hz}$	UA78L15C (legacy chip)	21	39	dB	
			UA78L15AC (legacy chip)	34	39		
		$V_I = 18.5\text{ V to }28.5\text{ V}$, and $f = 120\text{ Hz}$	UA78L15C (new chip)	40	45		
			UA78L15AC (new chip)	40	45		
Output voltage regulation	$T_J = 25^\circ\text{C}$	$I_O = 1\text{ mA to }100\text{ mA}$	for legacy chip		25	100	mV
		$I_O = 1\text{ mA to }40\text{ mA}$			15	75	
		$I_O = 1\text{ mA to }100\text{ mA}$	for new chip		25	27	
		$I_O = 1\text{ mA to }40\text{ mA}$			15	60	
Output noise voltage	$T_J = 25^\circ\text{C}$, and $f = 10\text{ Hz to }100\text{ kHz}$	for legacy chip		80		μV	
		for new chip		100			
Dropout voltage	$T_J = 25^\circ\text{C}$	for legacy chip		1.7		V	
		for new chip		1.7			
Quiescent current	$T_J = 25^\circ\text{C}$	for legacy chip		4.5	6.5	mA	
	$T_J = 125^\circ\text{C}$				8		
	$T_J = 25^\circ\text{C}$	for new chip		4.1	4.575		
	$T_J = 125^\circ\text{C}$				4.575		

6.13 Electrical Characteristics: UA78L15 (Both Legacy and New Chip) (continued)

at specified junction temperature, $V_i = 23\text{ V}$, $C_{DS} = 0.33\text{ }\mu\text{F}$, $C_{OUT} = 0.1\text{ }\mu\text{F}$ and $I_O = 40\text{ mA}$ (unless otherwise noted) ⁽¹⁾

PARAMETER	TEST CONDITIONS ⁽²⁾		MIN	TYP	MAX	UNIT
Line current change	$T_J = 0^\circ\text{C to } 125^\circ\text{C}$	$V_i = 15\text{ V to } 30\text{ V}$	legacy chip		1.5	mA
		$I_O = 1\text{ mA to } 40\text{ mA}$	UA78L15C (legacy chip)		0.2	
			UA78L15AC (legacy chip)		0.1	
	$T_J = -40^\circ\text{C to } 125^\circ\text{C}$	$V_i = 20\text{ V to } 30\text{ V}$	new chip		0.425	
		$I_O = 1\text{ mA to } 40\text{ mA}$	UA78L15C (new chip)		0.01	
			UA78L15AC (new chip)		0.02	

(1) Applies to UA78L15C and UA78L15AC.

(2) Pulsed-loading techniques maintain T_J as close to T_A as possible. Thermal effects must be taken into account separately. For legacy chip, temperature range for the UA78L15C, UA78L15AC is $T_J = 0^\circ\text{C to } 125^\circ\text{C}$. For new chip, temperature range for the UA78L15C and UA78L15AC is $T_J = -40^\circ\text{C to } 125^\circ\text{C}$.