

PIC16F18015/25/44/45 Full-Featured 8/14/20-Pin
Microcontrollers

PIC16F18015/25/44/45



Introduction

The PIC16F18076 microcontroller family has a suite of digital and analog peripherals that enable cost-sensitive sensor and real-time control applications. This product family is available from 8 to 44-pin packages in a memory range of 3.5 KB to 28 KB, with speeds up to 32 MHz. The family includes a 10-bit Analog-to-Digital Converter with Computation (ADCC), automated Capacitive Voltage Divider (CVD) techniques for advanced capacitive touch sensing, an 8-bit Digital-to-Analog Converter (DAC) module, and many more waveform control and communication peripherals. This small form factor, feature-rich device is well suited for low-cost sensor and control applications.

PIC16F18076 Family Summary

Table 1. Devices Included in This Data Sheet

Device	Program Flash Memory (bytes)	Data Flash Memory (EEPROM)(bytes)	Data SRAM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins ^{1/2} Peripheral Pin Select	8-Bit Timers with HL/T/ 16-Bit Timers(3)	10-Bit PWM/ CCP	10-Bit ADC Channels (External/Internal)	Charge Pump	PCON	EUSART	NCO	CWG	CUC	PVB	CMP	8-Bit DAC	ZCD	5V Bus Compatible I/O Pads	External Interrupt Pins	Interrupt-on-Change Pins	Watchdog Timer
PIC16F18015	14K	128	1024	YY	6/Y	3/3	3/2	5/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	6	Y
PIC16F18025	14K	128	1024	YY	12/Y	3/3	3/2	11/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	12	Y
PIC16F18044	7K	128	512	YY	18/Y	3/3	3/2	17/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	18	Y
PIC16F18045	14K	128	1024	YY	18/Y	3/3	3/2	17/4	1	2/2	2	1	1	4	2	1	1	1	Y	1	18	Y

Table 2. Devices Not Included in This Data Sheet

Device	Program Flash Memory (bytes)	Data Flash Memory (EEPROM)(bytes)	Data SRAM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins ^{1/2} Peripheral Pin Select	8-Bit Timers with HL/T/ 16-Bit Timers(3)	10-Bit PWM/ CCP	10-Bit ADC Channels (External/Internal)	Charge Pump	PCON	EUSART	NCO	CWG	CUC	PVB	CMP	8-Bit DAC	ZCD	5V Bus Compatible I/O Pads	External Interrupt Pins	Interrupt-on-Change Pins	Watchdog Timer
PIC16F18013	3.5K	128	256	YY	6/Y	3/3	3/2	5/4	1	1/1	1	1	0	4	2	1	1	1	Y	1	6	Y

continued																						
Device	Program Flash Memory (bytes)	Data Flash Memory (32K/64K/bytes)	Data SRAM (bytes)	Memory Access Partition/ Device Information Area	I/O Pins(I/O) Peripheral Pin Select	8-Bit Timers with HLT/ 16-Bit Timer0	10-Bit PWM/ CCP	10-Bit ADC Channels (External/Internal)	Charge Pump	PCON	USART	PICCO	CMO	CLE	PIA	CMP	8-Bit DAC	ECO	SMBus Compatible I/O Pins	External Interrupt Pins	Interrupt-on-Change Pins	Watchdog Timer
PIC16F18014	7K	128	512	YY	6/Y	3/3	3/2	3/4	1	1/1	1	1	0	4	2	1	1	1	Y	1	8	Y
PIC16F18023	1.5K	128	256	YY	12/Y	3/3	3/2	11/4	1	1/1	1	1	0	4	2	1	1	1	Y	1	12	Y
PIC16F18024	7K	128	512	YY	12/Y	3/3	3/2	11/4	1	1/1	1	1	0	4	2	1	1	1	Y	1	12	Y
PIC16F18025	28K	256	2048	YY	12/Y	3/3	3/2	11/4	1	1/2	2	1	1	4	2	1	1	1	Y	1	12	Y
PIC16F18046	28K	256	2048	YY	18/Y	3/3	3/2	17/4	1	1/2	2	1	1	4	2	1	1	1	Y	1	18	Y
PIC16F18054	7K	128	512	YY	25/Y	3/3	3/2	34/4	1	1/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18055	14K	128	1024	YY	25/Y	3/3	3/2	34/4	1	1/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18056	28K	256	2048	YY	25/Y	3/3	3/2	34/4	1	1/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18074	7K	128	512	YY	36/Y	3/3	3/2	35/4	1	1/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18075	14K	128	1024	YY	36/Y	3/3	3/2	35/4	1	1/2	2	1	1	4	2	1	1	1	Y	1	25	Y
PIC16F18026	28K	256	2048	YY	36/Y	3/3	3/2	35/4	1	1/2	2	1	1	4	2	1	1	1	Y	1	25	Y

Notes:

1. Total I/O count includes one input-only pin (MCLR).
2. Timer0 can be configured as either an 8 or 16-bit timer.

Core Features

- C Compiler Optimized RISC Architecture
- Operating Speed:
 - DC-32 MHz clock input
 - 125 ns minimum instruction time
- 16-Level Deep Hardware Stack
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR)
- Watchdog Timer (WDT)

Memory

- Up to 28 KB of Program Flash Memory
- Up to 2 KB of Data SRAM Memory
- Up to 256 Bytes of Data EEPROM Memory
- Memory Access Partition (MAP) with Program Flash Memory Partitioned into:
 - Application block
 - Boot block

- Storage Area Flash (SAF) block
- Programmable Code Protection and Write Protection
- Device Information Area (DIA) Stores:
 - Fixed Voltage Reference (FVR) measurement data
 - Microchip Unique Identifier (MUI)
- Device Characteristics Information (DCI) Stores:
 - Program/erase row sizes
 - Pin count details
- Direct, Indirect, and Relative Addressing Modes

Operating Characteristics

- Operating Voltage Range:
 - 1.8V to 5.5V
- Temperature Range:
 - Industrial: -40°C to 85°C
 - Extended: -40°C to 125°C

Power-Saving Functionality

- Sleep:
 - Reduce device power consumption
 - Reduce system electrical noise while performing ADC conversions
- Low Power Mode Features:
 - Sleep:
 - < 900 nA typical @ 3V/25°C (WDT enabled)
 - < 600 nA typical @ 3V/25°C (WDT disabled)
 - Operating Current:
 - 48 μ A typical @ 32 kHz, 3V/25°C
 - < 1 mA typical @ 4 MHz, 5V/25°C

Digital Peripherals

- Two Capture/Compare/PWM (CCP) Modules:
 - 16-bit resolution for Capture/Compare modes
 - 10-bit resolution for Pulse-Width Modulator (PWM) mode
- Three Pulse-Width Modulators (PWM):
 - 10-bit resolution
- Four Configurable Logic Cells (CLC):
 - Integrated combinational and sequential logic
- One Complimentary Waveform Generator (CWG):
 - Rising and falling edge dead-band control
 - Full-bridge, half-bridge, and 1-channel drive
 - Multiple signal sources
 - Programmable dead band
 - Fault-shutdown input
- One Configurable 8/15-Bit Timer (TMR0)

- Two 16-Bit Timers (TMR1/3) with Gate Control
- Three 8-Bit Timers (TMR2/4/6) with Hardware Limit Timer (HLT)
- One Numerically Controlled Oscillator (NCO):
 - Generates true linear frequency control and increased frequency resolution
 - Input clock up to 64 MHz
- Up to Two Enhanced Universal Synchronous Asynchronous Receiver Transmitters (EUSART):
 - RS-232, RS-485, and LIN compatible
 - Auto wake-up on Start
- Up to Two Host Synchronous Serial Ports (MSSP):
 - Serial Peripheral Interface (SPI) mode:
 - Client select synchronization
 - Inter-Integrated Circuit (I²C) mode:
 - 7/10-bit Addressing modes
- Peripheral Pin Select (PPS):
 - Enables pin mapping of digital I/O
- Device I/O Port Features:
 - Up to 35 I/O pins
 - One input-only pin
 - Individual I/O direction, open-drain, input threshold, slew rate, and weak pull-up control
 - Interrupt-on-Change (IOC) on up to 25 pins
 - One external interrupt pin

Analog Peripherals

- Analog-to-Digital Converter with Computation (ADCC):
 - 10-bit resolution
 - Up to 35 external input channels
 - Four internal input channels
 - Internal ADC oscillator (ADCRS)
 - Operates in Sleep
 - Selectable auto-conversion trigger sources
- Charge Pump Module:
 - Improves accuracy of analog modules at low voltages
- 8-Bit Digital-to-Analog Converter (DAC):
 - Output available on one I/O pin
 - Internal connections to ADC and Comparators
- One Comparator (CMP):
 - Up to four external inputs
 - Configurable output polarity
 - External output via Peripheral Pin Select
- Zero-Cross Detect (ZCD):
 - Detect when AC signal on pin crosses ground
- Two Fixed Voltage References (FVR):
 - Selectable 1.024V, 2.048V, and 4.096V output levels

- PVR1 internally connected to ADC
- PVR2 internally connected to Comparator and DAC

Clocking Structure

- High-Precision Internal Oscillator Block (HFINTOSC):
 - Selectable frequencies up to 32 MHz
 - $\pm 2\%$ at calibration
- Internal 31 kHz Oscillator (LFINTOSC)
- External High-Frequency Clock Input:
 - Two External Clock (EC) Power modes
- Secondary Oscillator (SOSC)

Programming/Debug Features

- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) with Three Breakpoints via Two Pins
- Debug Integrated On-Chip

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1. Packages

Table 1-1. Packages

Device	8-Pin PQFP	8-Pin SOIC	14-Pin PDIP	14-Pin SOIC	14-Pin TSSOP	16-Pin QFN	16-Pin VQFN	20-Pin PDIP	20-Pin SOIC	20-Pin SSOP	20-Pin QFN	20-Pin VQFN
PIC16F18015	•	•										
PIC16F18025			•	•	•	•	•					
PIC16F18044								•	•	•	•	•
PIC16F18045								•	•	•	•	•

2. Pin Diagrams

Figure 2-1. 8-Pin PDIP, SOIC



Figure 2-2. 14-Pin PDIP, SOIC, TSSOP

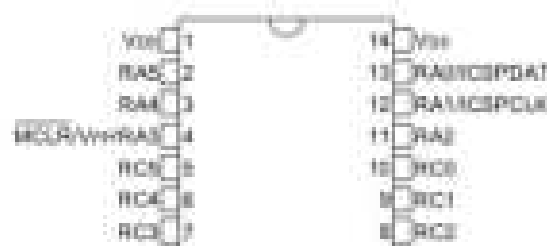
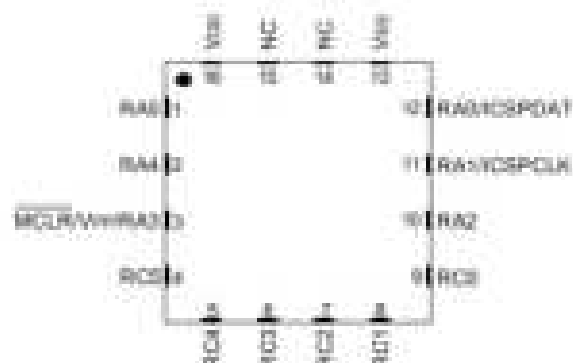


Figure 2-3. 16-Pin QFN, VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS} ; however, it must not be the only V_{SS} connection to the device.

Figure 2-4. 20-Pin PDIP, SOIC, SSOP

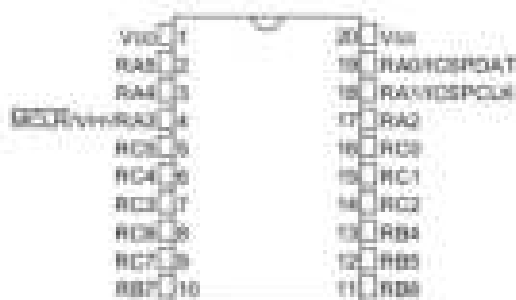
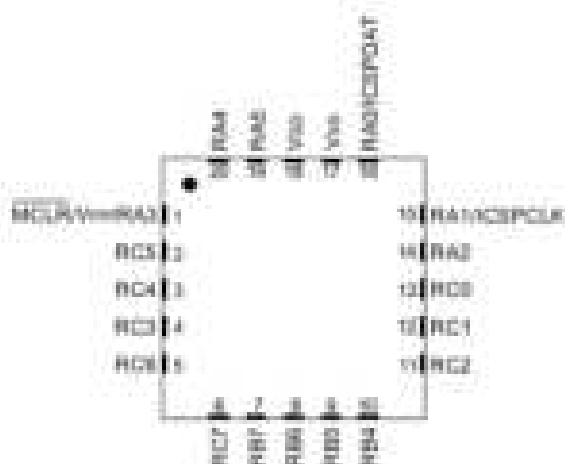


Figure 2-5. 20-Pin QFN, VQFN



Note: It is recommended that the exposed bottom pad be connected to V_{SS} ; however, it must not be the only V_{SS} connection to the device.

3. Pin Allocation Tables

Table 3-1. 8-Pin Allocation Table

IO	5-Pin PDIP SOT6	ADC	DAC	Comparator	ECG	Timers	CCP/PWM	CWG	CLC	MSSP	BUSART	IOC	Interrupt	Reset
RA0	7	ANAL	DAC1OUT1	COMP+	—	T3CK ⁽¹⁾ T3G ⁽¹⁾ 14N ⁽¹⁾	—	—	CLCIN1 ⁽²⁾	SCL1 ^(3,4) SDA1 ^(3,4) SDA2 ^(3,4) SDA3 ^(3,4) SDA4	DT1 ⁽⁴⁾ OC1 ^(3,4)	IOCA0	—	ICSPDAT ICSPDAT
RA1	6	ANAL VREF ⁽⁴⁾ (ADC)	DAC1REFH	COMP-	—	16N ⁽¹⁾	—	—	CLCIN2 ⁽²⁾	SCL1 ^(3,4) SDA1 ^(3,4)	DT1 ⁽⁴⁾ DT1 ⁽⁴⁾ OC2 ^(3,4) OC2 ^(3,4)	IOCA1	—	ICSPCLK ICSPCLK
RA2	5	ANAL	DAC1REFS	—	2CD1	T3CK ⁽¹⁾	—	CWG1 ^(1,4)	—	SDA3 ^(3,4) SDA4 ^(3,4)	—	IOCA2	INT ⁽¹⁾	—
RA3	4	—	—	—	—	—	—	—	CLCIN3 ⁽²⁾	—	—	IOCA3	—	WDR VREF
RA4	3	ANAL	—	COMP-	—	T3G ⁽¹⁾	—	—	—	—	—	IOCA4	—	CLROUT SOSC0
RA5	2	ANAL ADACT ⁽¹⁾	—	—	—	T3CK ⁽¹⁾ T2N ⁽¹⁾	CCP1 ⁽¹⁾ CCP2 ⁽¹⁾	—	CLCIN4 ⁽²⁾	—	—	IOCA5	—	CLIN SOSC1
VDD	1	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT ⁽²⁾	—	ADQADA ADQADB	—	COMP	—	TMR0	CCP1 CCP2 PWM3 PWM4 PWM5	CWG1A ⁽⁴⁾ CWG1B ⁽⁴⁾ CWG1C ⁽⁴⁾ CWG1D ⁽⁴⁾	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SCL1 SCL2 SDA1 SDA2 SCL3 ⁽⁴⁾ SCL4 ⁽⁴⁾ SDA3 ⁽⁴⁾ SDA4 ⁽⁴⁾	TX1 DT1 CK1 TX2 ⁽⁴⁾ DT2 ⁽⁴⁾ CK2 ⁽⁴⁾	—	—	

Notes:

1. This is a PPS-remappable input signal. The input function may be moved from the default location shown to any PORT's pin.
2. All output signals shown in this row are PPS-remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. Only available on the 8-pin PIC16F1815.

Table 3-2. 14/16-Pin Allocation Table

IO	14-Pin PDS-P SDIC TSSOP	16-Pin QFN VQFN	ADC	DAC	Comparator	SLD	Timers	CCP	CWG	CLC	MSP	USART	IOC	Interrupt	Basic
RA0	13	12	ANA0	DAC1OUT1	CTRS0+	—	—	—	—	—	SL1 ⁽¹⁾	—	IOCA0	—	ICSPDAT ICDDAT
RA1	12	11	ANA1 TempHADC	DAC1REF0+	CTRS0-	—	—	—	—	—	—	—	IOCA1	—	ICSPCLK ICDCLK
RA2	11	10	ANA2	DAC1REF0-	—	2CD1	TRC0 ⁽¹⁾	—	CWG1 ⁽¹⁾	—	—	—	IOCA2	W1 ⁽¹⁾	—
RA3	6	5	—	—	—	—	—	—	—	—	—	—	IOCA3	—	MCUR Vref
RA4	3	2	ANA4	—	—	—	TRG1 ⁽¹⁾	—	—	—	—	—	IOCA4	—	CLR01 ⁽¹⁾ SOSC0
RA5	2	1	ANA5	—	—	—	TRC0 ⁽¹⁾ TDA1 ⁽¹⁾	—	—	CLC0 ⁽¹⁾	—	—	IOCA5	—	CLR04 SOSC0
RC0	10	9	ANC0	—	—	—	—	—	—	—	SL1 ⁽¹⁾ ,A4 SD1 ⁽¹⁾ ,A4	CL2 ⁽¹⁾ ,A	IOCC0	—	—
RC1	9	8	ANC1	—	CTRS1	—	TDA1 ⁽¹⁾ TR	—	—	CLC0 ⁽¹⁾	SD0 ⁽¹⁾ ,A4 SD1 ⁽¹⁾ ,A4	W1 ⁽¹⁾ DT1 ⁽¹⁾ ,A	IOCC1	—	—
RC2	8	7	ANC2 ADAC0 ⁽¹⁾	—	CTRS0	—	TDA1 ⁽¹⁾ TR	—	—	—	—	—	IOCC2	—	—
RC3	7	6	ANC3	—	CTRS0-	—	—	CCP0 ⁽¹⁾	—	CLC0 ⁽¹⁾	W1 ⁽¹⁾	—	IOCC3	—	—
RC4	6	5	ANC4	—	—	—	TRG1 ⁽¹⁾	—	—	CLC0 ⁽¹⁾	SL2 ⁽¹⁾ ,A4 SD2 ⁽¹⁾ ,A4	CL1 ⁽¹⁾ ,A	IOCC4	—	—
RC5	5	4	ANC5	—	—	—	TRC0 ⁽¹⁾	CCP1 ⁽¹⁾	—	—	SD0 ⁽¹⁾ ,A4 SD1 ⁽¹⁾ ,A4 SD2 ⁽¹⁾ ,A4	W1 ⁽¹⁾ DT1 ⁽¹⁾ ,A	IOCC5	—	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	VSS
OUT ⁽²⁾	—	—	ADURDA ADGRDS	—	COMP	—	TRRS	CCP1 CCP2 PWM0 PWM1 PWM5	CWG1A CWG1B CWG1C CWG1D	CLC1OUT CLC2OUT CLC3OUT CLC4OUT	SL1 SD1 SD41 SD01 SL2 SD42 SD43 SD02	TR1 DT1 CR1 TR2 DT2 CR2	—	—	—

Notes:

1. This is a PPS-remappable input signal. The input function may be moved from the default location shown to any PORT's pin.
2. All output signals shown in this row are PPS-remappable.
3. This is a bidirectional signal. For normal operation, user software must map this signal to the same pin via the PPS input and PPS output registers.
4. These pins can be configured for I²C or SMBus logic levels via the KeyIO registers. The SCI1/SCI4 signals may be assigned to these pins for expected operation. PPS assignments of these signals to other pins will operate; however, the logic levels will be standard TTL/5V as selected by the RGLVL register.