nRF51822

Multiprotocol *Bluetooth*® low energy/2.4 GHz RF System on Chip

Product Specification v3.4

Key Features

- 2.4 GHz transceiver
  - -93 dBm sensitivity in *Bluetooth*® low energy mode
  - 250 kbps, 1 Mbps, 2 Mbps supported data rates
  - TX Power -20 to +4 dBm in 4 dB steps
  - TX Power -30 dBm Whisper mode
  - 13 mA peak RX, 10.5 mA peak TX (0 dBm)
  - 9.7 mA peak RX, 8 mA peak TX (0 dBm) with DC/DC
  - RSSI (1 dB resolution)
- ARM® Cortex™-M0 32 bit processor
  - 275 µA/MHz running from flash memory
  - 150 µA/MHz running from RAM
  - Serial Wire Debug (SWD)
- S100 series SoftDevice ready
- Memory
  - 256 kB or 128 kB embedded flash program memory
  - 16 kB or 32 kB RAM
- On-air compatibility with nRF24L series
- Flexible Power Management
  - Supply voltage range 1.8 V to 3.6 V
  - 4.2 µs wake-up using 16 MHz RC OSC
  - 0.6 µA at 3 V OFF mode
  - 1.2 µA at 3 V in OFF mode + 1 region RAM retention
  - 2.6 µA at 3 V ON mode, all blocks IDLE
- 8/9/10 bit ADC - 8 configurable channels
- 31 General Purpose I/O Pins
- One 32 bit and two 16 bit timers with counter mode
- SPI Master/Slave
- Low power comparator
- Temperature sensor
- Two-wire Master (I2C compatible)
- UART (CTS/RTS)
- CPU independent Programmable Peripheral Interconnect (PPI)
- Quadrature Decoder (QDEC)
- AES HW encryption
- Real Timer Counter (RTC)
- Package variants
  - QFN48 package, 6 x 6 mm
  - WLCSP package, 3.50 x 3.83 x 0.50 mm
  - WLCSP package, 3.50 x 3.83 x 0.35 mm
  - WLCSP package, 3.83 x 3.83 x 0.50 mm
  - WLCSP package, 3.83 x 3.83 x 0.35 mm
  - WLCSP package, 3.50 x 3.33 x 0.50 mm

Applications

- Computer peripherals and I/O devices
  - Mouse
  - Keyboard
  - Multi-touch trackpad
- Interactive entertainment devices
  - Remote control
  - Gaming controller
- Beacons
- Personal Area Networks
  - Health/fitness sensor and monitor devices
  - Medical devices
  - Key fobs + wrist watches
- Remote control toys

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Contact details

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Information regarding product updates, downloads, and technical support can be accessed through your My Page account on our home page.

Main office: Otto Nielsens veg 12
7052 Trondheim
Norway
Phone: +47 72 89 89 00
Fax: +47 72 89 89 89

Mailing address: Nordic Semiconductor
P.O. Box 2336
7004 Trondheim
Norway

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Datasheet Status

Status	Description
Objective Product Specification (OPS)	This product specification contains target specifications for product development.
Preliminary Product Specification (PPS)	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product Specification (PS)	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Revision History

Date	Version	Description
April 2021	3.4	**Updated content:** • *Section 10.7 "Product options"* on page 78
July 2016	3.3	Added documentation for the nRF51822 CTAA version of the chip. **Added content:** • *Section 8.3 "CTAA WLCSP package"* on page 71 • *Section 11.9 "CTAA WLCSP package"* on page 118 **Updated content:** • Feature list on the front page • *Section 3.2.3 "CEAA, CTAC, CTAA, and CTAC WLCSP ball assignment and functions"* on page 17 • *Section 3.2.1 "Code organization"* on page 22 • *Section 3.2.2 "RAM organization"* on page 22 • *Section 3.3 "Memory Protection Unit (MPU)"* on page 23 • *Section 7.1.2 "CTAA and CTAC light sensitivity"* on page 38 • *Section 7.2 "CTAA and CTAC mechanical strength"* on page 39 • *Section 10.6 "Code ranges and values"* on page 76 • *Section 10.7 "Product options"* on page 78 • *Chapter 11 "Reference circuitry"* on page 79. Added resistor R1 on the schematics for all variants.

Date	Version	Description
January 2016	3.3	Added documentation for the nRF51822 CTAC version of the chip. **Added content:** • *Section 4.10.1 "Enable 4 Mbps SPIS bit rate"* on page 35 • *Section 7.2 "CTAA and CTAC mechanical strength"* on page 39 • *Section 9.8 "CTAC WLCSP package"* on page 72 • *Section 11.1d "CTAC WLCSP package"* on page 126 **Updated content:** • Feature list on the front page. • *Section 2.2.3 "CEAA, CFAC, CTAA, and CTAC WLCSP ball assignment and functions"* on page 17 • *Section 3.2.1 "Code organization"* on page 22 • *Section 3.2.2 "RAM organization"* on page 23 • *Section 3.3 "Memory Protection Unit (MPU)"* on page 23 • *Chapter 6 "Absolute maximum ratings"* on page 38 • *Section 7.1 "WLCSP light sensitivity"* on page 39 • *Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"* on page 41 • *Section 8.1.3 "32.768 kHz crystal oscillator (32K XOSC)"* on page 43 • *Section 8.1.4 "32.768 kHz RC oscillator (32K RCOSC)"* on page 44 • *Section 8.2 "Power management"* on page 45 • *Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"* on page 57 • *Section 10.6 "Code ranges and values"* on page 76 • *Section 10.7 "Product options"* on page 78
October 2014	3.1	Added documentation for the following versions of the chip: • nRF51822-QFAC Aa0 • nRF51822-QFAC Aa0 • nRF51822-CDAB Aa0 • nRF51822-CDAB Aa0 • nRF51822-CFAC Aa0 • nRF51822-CFAC Aa0 (The x in the build codes can be any number between 0 and 9.) **Added content:** • *Section 2.2.2 "CDAB WLCSP ball assignment and functions"* on page 14 • *Section 9.2 "CDAB WLCSP package"* on page 68 • *Section 9.4 "CFAC WLCSP package"* on page 70 **Updated content:** • Feature list on the front page. • *Section 2.2.3 "CEAA and CFAC WLCSP ball assignment and functions"* on page 17 • *Section 3.2.1 "Code organization"* on page 22 • *Section 3.2.2 "RAM organization"* on page 22 • *Section 3.3 "Memory Protection Unit (MPU)"* on page 23 • *Section 8.2 "Power management"* on page 43 • *Section 8.3 "Block resource requirements"* on page 48 • *Section 8.12 "Analog to Digital Converter (ADC) specifications"* on page 61 • *Section 10.6 "Code ranges and values"* on page 76 • *Section 10.7 "Product options"* on page 78

Date	Version	Description
August 2014	3.0	Update to reflect the changes in build code: • nRF51822-QFAA Hx0 • nRF51822-QFAA Ex0 • nRF51822-QFAB Cx0 (The x in the build codes can be any number between 0 and 9.) If you are working with a previous revision of the chip, read version 2.a of the document. **Added content:** • *Section 8.5.3 "Radio current consumption with DC/DC enabled"* on page 51 • *Section 11.1.1 "PCB layout example"* on page 80 **Updated content:** • Feature list on the front page. • *Section 2.1 "Block diagram"* on page 11 • *Section 3.2.1 "Code organization"* on page 22 • *Section 3.2.2 "RAM organization"* on page 22 • *Section 3.3 "Memory Protection Unit (MPU)"* on page 23 • *Section 3.4 "Power management (POWER)"* on page 24 • *Section 3.6 "Clock management (CLOCK)"* on page 28 • *Section 3.8 "Debugger support"* on page 31 • *Section 4.2 "Timer/counters (TIMER)"* on page 33 • *Chapter 5 "Instance table"* on page 37 • *Chapter 7 "Operating conditions"* on page 39 • *Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"* on page 41 • *Section 8.1.3 "32 MHz crystal oscillator (32M XOSC)"* on page 42 • *Section 8.1.4 "16 MHz RC oscillator (16M RCOSC)"* on page 43 • *Section 8.1.6 "32.768 kHz RC oscillator (32k RCOSC)"* on page 44 • *Section 8.1.7 "32.768 kHz Synthesized oscillator (32k SYNT)"* on page 44 • *Section 8.2 "Power management"* on page 48 • *Section 8.3 "Block resource requirements"* on page 49 • *Section 8.4 "CPU"* on page 49 • *Section 8.5.6 "Radio timing parameters"* on page 55 • *Section 8.5.7 "Antenna matching network requirements"* on page 55 • *Section 8.7 "Universal Asynchronous Receiver/Transmitter (UART) specifications"* on page 56 • *Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"* on page 57 • *Section 8.12 "Analog to Digital Converter (ADC) specifications"* on page 61 • *Section 8.13 "Timer (TIMER) specifications"* on page 62 • *Section 8.15 "Temperature sensor (TEMP)"* on page 62 • *Section 8.22 "Non-Volatile Memory Controller (NVMC) specifications"* on page 63 • *Section 8.24 "Low Power Comparator (LPCOMP) specifications"* on page 66 • *Section 9.2 "CDAB WLCSP package"* on page 68 • *Section 10.7.2 "Development tools"* on page 78 • *Chapter 11 "Reference circuitry"* on page 79

Date	Version	Description
October 2013	3.0	This version of the document will target the nRF51822 QFAA G0 revision of the chip. If you are working with a previous revision of the chip, read version 1.3 or earlier of the document. **Updated** the following sections: Key Feature list on the front page. *Chapter 1 "Introduction"* on page 10. *Section 2.1 "Block diagram"* on page 11. *Section 2.2 "Pin assignments and functions"* on page 12. *Section 3.2 "Memory"* on page 21. *Section 3.5 "Programmable Peripheral Interconnect (PPI)"* on page 27. *Section 3.7 "GPIO"* on page 31. *Section 4.1 "2.4 GHz radio (RADIO)"* on page 32. *Section 4.2 "Timer/counters (TIMER)"* on page 33. *Section 4.3 "Real Time Counter (RTC)"* on page 33. *Section 4.10 "Serial Peripheral Interface (SPI/SPIS)"* on page 35. *Section 4.12 "Universal Asynchronous Receiver/Transmitter (UART)"* on page 36. *Section 4.14 "Analog to Digital Converter (ADC)"* on page 36. *Section 4.15 "GPIO Task Event blocks (GPIOTE)"* on page 36. *Chapter 5 "Instance table"* on page 37. *Chapter 6 "Absolute maximum ratings"* on page 38. *Chapter 7 "Electrical specifications"* on page 40. *Section 8.1 "Clock sources"* on page 40. *Section 8.1.2 "16 MHz crystal oscillator (16M XOSC)"* on page 41. *Section 8.1.3 "32 MHz crystal oscillator (32M XOSC)"* on page 42. *Section 8.2 "Power management"* on page 43. *Section 8.3 "Block resource requirements"* on page 49. *Section 8.7 "Universal Asynchronous Receiver/Transmitter (UART) specifications"* on page 56. *Section 8.8 "Serial Peripheral Interface (SPI) Master specifications"* on page 58. *Section 8.11 "GPIO Tasks and Events (GPIOTE) specifications"* on page 60. *Section 8.13 "Timer (TIMER) specifications"* on page 62. *Section 8.16 "Random Number Generator (RNG) specifications"* on page 63. *Section 8.17 "AES Electronic Codebook Mode Encryption (ECB) specifications"* on page 63. *Section 8.18 "AES CCM Mode Encryption (CCM) specifications"* on page 63. *Section 8.19 "Accelerated Address Resolver (AAR) specifications"* on page 63. *Section 8.21 "Quadrature Decoder (QDEC) specifications"* on page 64. *Section 11.1 "PCB guidelines"* on page 79. *Section 11.3 "QFAA QFN48 package"* on page 82, and *Section 11.7 "CEAA WLCSP package"* on page 106. **Added** the following sections: *Section 3.3 "Memory Protection Unit (MPU)"* on page 23. *Section 4.5 "AES CCM Mode Encryption (CCM)"* on page 34. *Section 4.6 "Accelerated Address Resolver (AAR)"* on page 34. *Section 4.16 "Low Power Comparator (LPCOMP)"* on page 36. *Section 8.5.7 "Antenna matching network requirements"* on page 55. *Section 8.8 "Serial Peripheral Interface Slave (SPIS) specifications"* on page 57. *Section 8.18 "AES CCM Mode Encryption (CCM) specifications"* on page 63. *Section 8.19 "Accelerated Address Resolver (AAR) specifications"* on page 63, and *Section 8.24 "Low Power Comparator (LPCOMP) specifications"* on page 66.
May 2013	1.3	Updated schematics and BOMs in section 11.3 on page 81.

Date	Version	Description
April 2015	3.2	Added chip variant nRF51822-CEAA. Updated feature list on front page. **Updated** Section 3.2.1 on page 15, Section 3.2.2 on page 15, Chapter 6 on page 38, Section 10.4 on page 52, and Section 10.5.1 on page 53. **Added** Section 2.2.2 on page 10, Section 7.1 on page 28, Section 9.2 on page 30, and Section 11.3 on page 61. **Removed** PCB layouts in Chapter 11 on page 54.
March 2013	3.1	Added chip variant nRF51822-QFAB. Added 32 MHz crystal oscillator feature. Updated feature list on front page. Moved subsection 'Calculating current when the DC/DC converter is enabled' from chapter 6 to the nRF51 Series Reference Manual. **Updated** Chapter 1 on page 6, Section 2.2 on page 8, Section 5.2 on page 12, Section 3.5 on page 16, Section 3.5.1 on page 17, Section 4.2 on page 21, Chapter 5 on page 24, Section 6.1 on page 27, Section 6.1.2 on page 28, Section 6.1.5 on page 30, Section 6.2 on page 32, Section 6.3 on page 34, Section 6.5.3 on page 36, Section 6.6 on page 40, Section 6.9 on page 41, Section 6.10 on page 42, Section 6.14 on page 43, Chapter 10 on page 47, Section 11.2 on page 51, Section 11.3 on page 54, and Section 11.4 on page 57. **Added** Section 3.5.4 on page 18, Section 6.1.3 on page 29, and Section 11.1 on page 50.
November 2012	3.0	**Changed from PPS to PS. Updated the feature list on the front page.** **Updated** Table 11 on page 25, Table 12 on page 26, Table 14 on page 28, Table 15 on page 28, Table 16 on page 29, Table 17 on page 29, Table 18 on page 30, Table 19 on page 31, Table 21 on page 32, Table 22 on page 33, Table 25 on page 33,Table 27 on page 36, Table 28 on page 37, Table 29 on page 37, Table 31 on page 38, Table 32 on page 38, Table 35 on page 39, Table 38 on page 40, Table 39 on page 40, Table 50 on page 47, Figure 9 on page 46, and Table 57 on page 50.

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1 Introduction

The nRF51822 chip is an ultra-low power 2.4 GHz wireless System on Chip (SoC) integrating the nRF51 Series 2.4 GHz transceiver, a 32 bit ARM® Cortex™-M0 CPU, flash memory, and analog and digital peripherals. nRF51822 can support Bluetooth® low energy and a range of proprietary 2.4 GHz protocols, such as Gazell from Nordic Semiconductor.

Fully qualified Bluetooth low energy stacks for nRF51822 are implemented in the S100 series of SoftDevices. The S100 series of SoftDevices are available for free and can be downloaded and installed on nRF51822 independent of your own application code.

1.1 Required reading

The following documentation is available for download from our Infocenter:

- *nRF51 Series Reference Manual*
- *nRF51822-PAN (Product Anomaly Notification)*
- *PCN-092 (nRF51822 Product Change Notification)*

1.2 Writing conventions

This product specification follows a set of typographic rules to ensure that the document is consistent and easy to read. The following writing conventions are used:

- Command, event names, and bit state conditions, are written in `Lucida Console`.
- Pin names and pin signal conditions are written in **Consolas**.
- File names and User Interface components are written in **bold**.
- Internal cross references are italicized and written in ***semi-bold***.
- Placeholders for parameters are written in *italic* regular text font. For example, a syntax description of Connect will be written as:
  Connect(*TimeOut*, *AdvInterval*).
- Fixed parameters are written in regular text font. For example, a syntax description of Connect will be written as:
  Connect(0x00F0, *Interval*).

2 Product overview

2.1 Block diagram

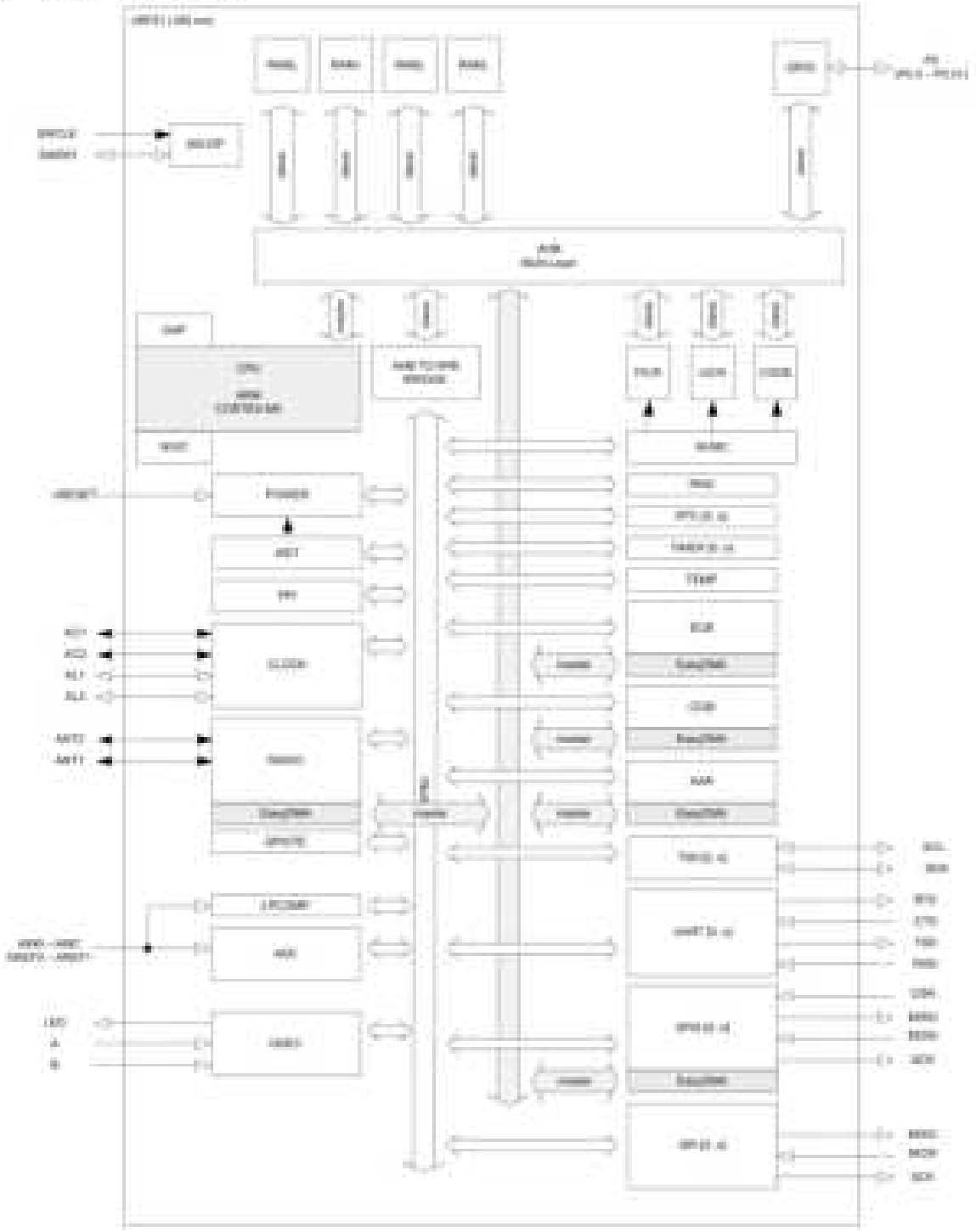


Figure 1 Block diagram

2.2 Pin assignments and functions

This section describes the pin assignment and the pin functions.

2.2.1 Pin assignment QFN48

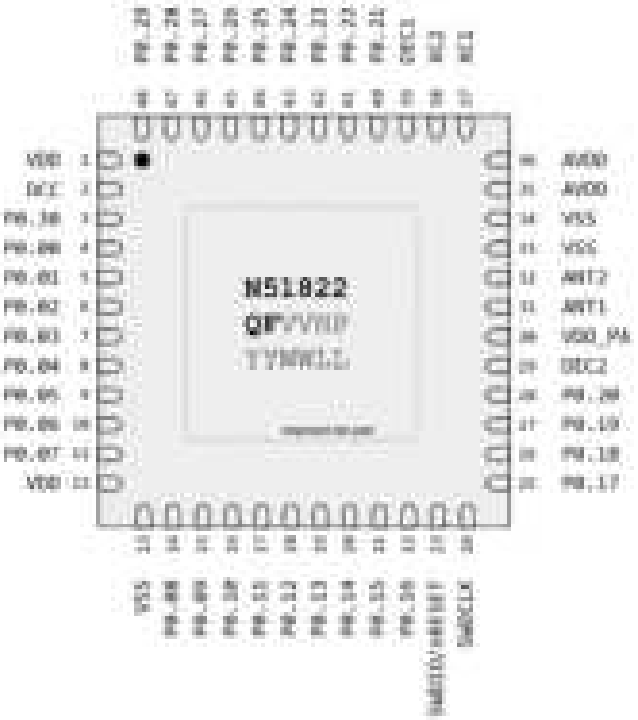


Figure 2 Pin assignment - QFN48 package

Note: VV = Variant code, HP = Build code, YYWWLL = Tracking code.
For more information, see *Section 10.6 "Code ranges and values"* on page 76.