



SN74LVC1GU04 Single Inverter Gate

1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Unbuffered Output
- Maximum t_{pd} of 3.7 ns at 3.3 V
- Low Power Consumption, 10- μ A Maximum I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{OL} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JEDEC 78, Class II
- ESD Protection Exceeds JEDEC 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

2 Applications

- AV Receivers
- Blu-ray Players and Home Theaters
- DVD Recorders and Players
- Desktop or Notebook PCs
- Digital Radio or Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PCs
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Pro Audio Mixers
- Smoke Detectors
- Solid-State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablets: Enterprise
- Audio Docks: Portable
- DLP Front Projection Systems
- DVR and DVS
- Digital Picture Frame (DPF)
- Digital Still Cameras

3 Description

This single inverter gate is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1GU04 device contains one inverter with an unbuffered output and performs the Boolean function $Y = A$.

NanoFree package technology is a major breakthrough in device packaging concepts, using the die as the package.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1GU04DBV	SOT-23 (5)	2.90 mm × 1.60 mm
SN74LVC1GU04DCK	SC70 (5)	2.00 mm × 1.25 mm
SN74LVC1GU04DRL	SOT-SX3 (5)	1.60 mm × 1.20 mm
SN74LVC1GU04DRY	SON (6)	1.45 mm × 1.00 mm
SN74LVC1GU04DSF	SON (6)	1.00 mm × 1.00 mm
SN74LVC1GU04YZP	DSSGA (5)	1.44 mm × 0.94 mm
SN74LVC1GU04YZV	DSSGA (4)	0.91 mm × 0.91 mm
SN74LVC1GU04DPW	X2SON (5)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision X (November 2017) to Revision Y

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• Updated input voltage minimum from 0.5 V to -0.5 V in Absolute Maximum Ratings table.....	5
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Changes from Revision W (January 2016) to Revision X

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• Changed values in the Thermal Information table to align with JEDEC standards.....	6
• Updated Feature Description to include more detailed information about specific device features.....	9
• Changed Typical Application to oscillator circuit.....	11
• Added DPM layout example.....	13

Changes from Revision V (November 2013) to Revision W

	Page
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• Added Applications section, Device Information table, ESD Ratings table, Thermal Information table, Typical Characteristics, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section.....	1
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Changes from Revision U (June 2011) to Revision V

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• Updated document to new TI data sheet format.....	1
• Updated operating free-air temperature range in Recommended Operating Conditions table.....	5

5 Pin Configuration and Functions



Pin Functions ⁽¹⁾⁽²⁾

NAME	PIN		IO	DESCRIPTION
	DBV, DRL, OCK, DPW	YZV		
A	2	A1	I	Input
GND	3	B1	—	Ground
NC	1	—	—	Not connected
V _{CC}	5	A2	—	Positive Supply
Y	4	B2	O	Output

(1) NC – No internal connection.

(2) See Mechanical Packaging and Orderable Information for dimensions.

SN74LVC1GU04

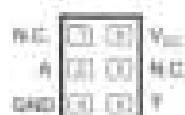
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DSP Package
6-Pin SOH
Top View



DRY Package
6-Pin SOH
Top View



YZP Package
6-Pin DSBGA
Top View



GND -- Do not use

Pin Functions⁽¹⁾⁽²⁾

NAME	PIN		I/O	DESCRIPTION
	DSP, DRY	YZP		
A	2	B1	I	Input
GND	3	C1	—	Ground
NC	1, 5	A1, B2	—	Not connected
V _{CC}	6	A2	—	Positive Supply
Y	4	C2	O	Output

(1) NC -- No internal connection

(2) See Mechanical Packaging and Ordering Information for dimensions

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.5	6.5	V
V_i	Input voltage ⁽²⁾	-0.5	6.5	V
V_O	Voltage applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{in}	Input clamp current		-60	mA
I_{op}	Output clamp current		-60	mA
I_O	Continuous output current		±60	mA
	Continuous current through V_{CC} or GND		±100	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in Recommended Operating Conditions.

6.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁴	±1000

6.3 Recommended Operating Conditions

See ⁽¹⁾.

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.65	5.5	V
V_{IH}	High-level input voltage	$I_O = -100 \mu A$	$0.75 \times V_{CC}$	V
V_{IL}	Low-level input voltage	$I_O = 100 \mu A$	$0.25 \times V_{CC}$	V
V_i	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 1.65 V$	-4	mA
		$V_{CC} = 2.5 V$	-8	
		$V_{CC} = 3 V$	-16	
		$V_{CC} = 4.5 V$	-24	
		$V_{CC} = 5.5 V$	-32	
I_{OL}	Low-level output current	$V_{CC} = 1.65 V$	4	mA
		$V_{CC} = 2.5 V$	8	
		$V_{CC} = 3 V$	16	
		$V_{CC} = 4.5 V$	24	
		$V_{CC} = 5.5 V$	32	
T_A	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. For more information, see the Implications of Stuck or Floating CMOS Inputs application report.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC1G04								UNIT
		DBV (SOT-23)	OCK (SC78)	ORL (SOT-563)	ORY (SON)	OSP (SON)	OPW (X2SON)	YZV (DSBGA)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	5 PINS	5 PINS	5 PINS	4 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	231.5	270.1	256.2	369.8	410.3	611	165.2	144.4	°C/W
$R_{\theta JCASE}$	Junction-to-case (top) thermal resistance	138.4	170.9	157.3	257.8	208.4	241.9	2.1	1.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.1	70.9	145.3	230.8	262.6	374.2	55.9	39.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	45.2	47	14.7	77.2	36	46	1.1	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.7	69.3	145.9	231	262.3	373.3	56.3	39.7	°C/W
$R_{\theta JCBOT}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	165.0	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{OH}	High-level output voltage	$V_{OH} = 3\text{ V}$, $I_{OH} = -100\text{ }\mu\text{A}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V	$V_{OH} = 0.1$	0.1	V
		$V_{OH} = 3\text{ V}$, $I_{OH} = -4\text{ mA}$, $V_{DD} = 1.8\text{ V}$	1.3		
		$V_{OH} = 3\text{ V}$, $I_{OH} = -8\text{ mA}$, $V_{DD} = 2.3\text{ V}$	1.6		
		$V_{OH} = 3\text{ V}$, $I_{OH} = -16\text{ mA}$, $V_{DD} = 3\text{ V}$	2.4		
		$V_{OH} = 3\text{ V}$, $I_{OH} = -24\text{ mA}$, $V_{DD} = 3\text{ V}$	2.3		
		$V_{OH} = 3\text{ V}$, $I_{OH} = -42\text{ mA}$, $V_{DD} = 4.5\text{ V}$	3.8		
		$V_{OH} = V_{DD}$, $I_{OH} = 100\text{ }\mu\text{A}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V	0.1		
V_{OL}	Low-level output voltage	$V_{OH} = V_{DD}$, $I_{OL} = 4\text{ mA}$, $V_{DD} = 1.8\text{ V}$	0.45	0.45	V
		$V_{OH} = V_{DD}$, $I_{OL} = 8\text{ mA}$, $V_{DD} = 2.3\text{ V}$	0.3		
		$V_{OH} = V_{DD}$, $I_{OL} = 16\text{ mA}$, $V_{DD} = 3\text{ V}$	0.4		
		$V_{OH} = V_{DD}$, $I_{OL} = 24\text{ mA}$, $V_{DD} = 3\text{ V}$	0.55		
		$V_{OH} = V_{DD}$, $I_{OL} = 32\text{ mA}$, $V_{DD} = 4.5\text{ V}$	0.55		
		$V_{OH} = V_{DD}$, $I_{OL} = 100\text{ }\mu\text{A}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V	0.1		
		$V_{OH} = V_{DD}$, $I_{OL} = 100\text{ }\mu\text{A}$, $V_{DD} = 1.8\text{ V}$ to 5.5 V	0.1		
I_I	Input leakage current	A input: $V_I = 3.5\text{ V}$ or GND, $V_{DD} = 3\text{ V}$ to 5.5 V		25	μA
I_{DD}	Supply current	$V_I = 3.5\text{ V}$ or GND, $I_I = 0$, $V_{DD} = 1.8\text{ V}$ to 5.5 V		10	μA
C_i	Input capacitance	$V_I = V_{DD}$ or GND, $V_{DD} = 3.5\text{ V}$, $T_A = -40^{\circ}\text{C}$ to 85°C	7		pF

(1) All typical values are at $V_{DD} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$.

6.6 Switching Characteristics: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

over recommended operating free-air temperature range (unless otherwise noted) (See Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
t_{pd} Propagation delay	A-to-Y	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	1.3	5	ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1	4	
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.1	3.7	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1	3	

6.7 Switching Characteristics: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$

over recommended operating free-air temperature range (unless otherwise noted) (See Figure 2)

PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
t_{pd} Propagation delay	A-to-Y	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	1.3	5.5	ns
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	1	4.5	
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.1	4.2	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	1	3.5	

6.8 Operating Characteristics

$T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS		TYP	UNIT
C_{PD} Power dissipation capacitance	$f = 10\text{ MHz}$	$V_{CC} = 1.8\text{ V}$	8	pF
		$V_{CC} = 2.5\text{ V}$	11	
		$V_{CC} = 3.3\text{ V}$	13	
		$V_{CC} = 5\text{ V}$	27	

6.9 Typical Characteristic

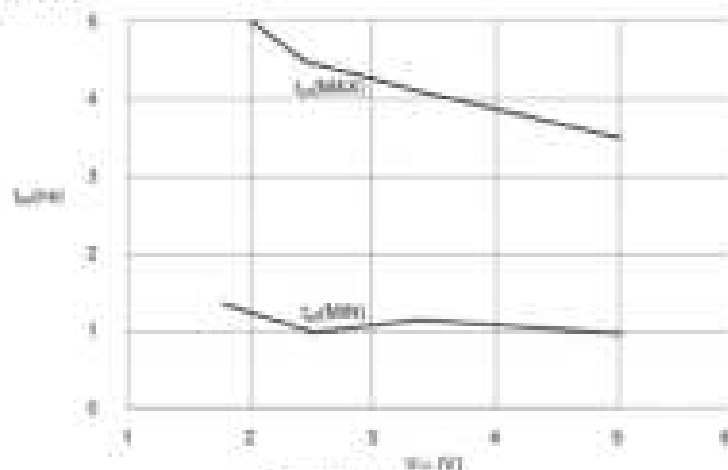
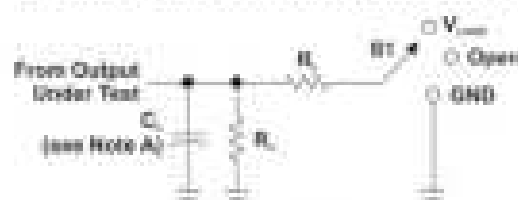


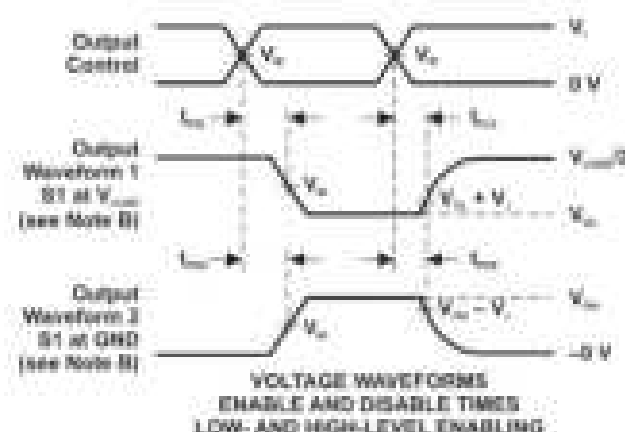
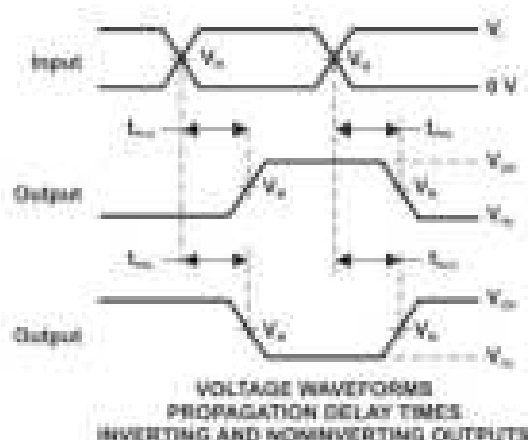
Figure 1. t_{pd} vs V_{CC}

7 Parameter Measurement Information


LOAD CIRCUIT

TEST	S1
t_{LH}/t_{HL}	Open
t_{LH}/t_{HL}	V_{DD}
t_{LH}/t_{HL}	GND

V_{DD}	INPUTS		V_{OL}	V_{OH}	C_L	R_L	V_I
	V_I	t_A					
1.5 V ± 0.15 V	V_{DD}	±2 ns	$V_{DD}/2$	$1 \times V_{DD}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{DD}	±2 ns	$V_{DD}/2$	$1 \times V_{DD}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	1 V	±2.5 ns	1.5 V	0 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{DD}	±2.5 ns	$V_{DD}/2$	$1 \times V_{DD}$	50 pF	500 Ω	0.3 V



- NOTES:**
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, $Z_o = 50 \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{LH} and t_{HL} are the same as t_L .
 - t_{LH} and t_{HL} are the same as t_L .
 - t_{LH} and t_{HL} are the same as t_L .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVC1GU04 device contains one inverter with an unbuffered output with a maximum sink current of 32 mA.

8.2 Functional Block Diagram



Figure 3. Logic Diagram (Positive Logic)

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high-drive capability of this device creates fast edges into light loads, so routing and load conditions must be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the power output of the device to be limited to avoid thermal runaway and damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

8.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst-case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law ($R = V / I$).

Signals that are applied to the inputs need to have fast edge rates, as shown by $\Delta t_{0.5}$ in the *Recommended Operating Conditions*, to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

8.3.3 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as shown in Figure 4.

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

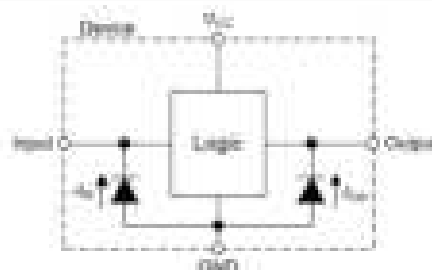


Figure 4. Electrical Placement of Clamping Diodes for Each Input and Output

Feature Description (continued)

8.3.4 Partial Power Down (I_{leak})

The inputs and outputs for this device enter a high-impedance state when the supply voltage is 0 V. The maximum leakage into or out of any input or output pin on the device is specified by I_{leak} in the *Electrical Characteristics*.

8.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

8.3.6 Unbuffered Logic

A standard CMOS logic function typically consists of at least three stages: the input inverter, the logic function, and the output inverter. Some devices have multiple stages at the input or output for various reasons. An unbuffered CMOS logic function eliminates the extra input and output stages; the device only contains the required logic function which is directly driven from the inputs and directly drives the outputs.

The unbuffered inverter is commonly used in oscillator circuits because it is less sensitive to parameter changes in the oscillator circuit due to having lower total gain than a buffered equivalent. To learn more about how to use an unbuffered inverter in an oscillator circuit, see *Use of the CMOS Unbuffered Inverter in Oscillator Circuits*.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVC1GU04.

Table 1. Function Table

INPUT A	OUTPUT Y
H	L
L	H

9 Application and Implementation

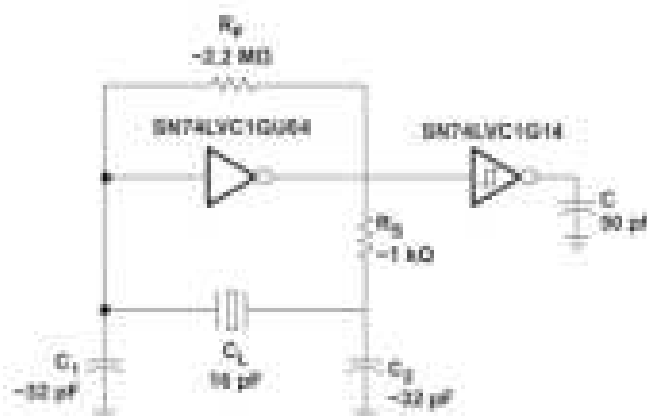
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The unbuffered inverter is commonly used in oscillator circuits because it is less sensitive to parameter changes in the oscillator circuit due to having lower total gain than a buffered equivalent. An example application circuit is shown in Figure 5. To learn more about how to use an unbuffered inverter in an oscillator circuit, refer to the *Use of the CMOS Unbuffered Inverter in Oscillator Circuits* application report.

9.2 Typical Application



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Figure 5. Typical Application Diagram

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive also creates fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

To learn more about how to use an unbuffered inverter in an oscillator circuit, refer to the *Use of the CMOS Unbuffered Inverter in Oscillator Circuits* application report.

1. Recommended Input Conditions

- Specified high and low levels. See (V_{IH} and V_{IL}) in Recommended Operating Conditions.
- Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in Recommended Operating Conditions at any valid V_{CC} .

2. Absolute Maximum Output Conditions

- Load currents must not exceed (I_O max) per output and must not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in Absolute Maximum Ratings.
- Outputs must not be pulled above the voltage rated in the Absolute Maximum Ratings.

Typical Application (continued)

9.2.3 Application Curve

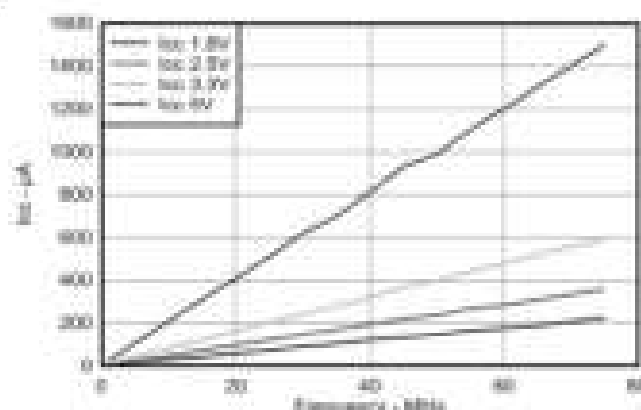


Figure 8. I_{CC} vs Frequency

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the Recommended Operating Conditions table.

The V_{CC} pin must have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended, and it is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.